Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-7 (Canceled)

Claim 8 (Currently amended): A method of producing multiple MEMS device packages, ~~a MEMS device package,~~ the method comprising single wafer patterning steps and batch processing steps performed on a cap wafer wherein all single wafer patterning steps performed on the cap wafer precede the batch processing steps, the single wafer patterning steps comprising: ~~of:~~

providing the cap wafer with ~~a semiconductor wafer having~~ first and second oxide layers on oppositely-disposed first and second surfaces, respectively, thereof;

depositing first and second masking layers on the first and second oxide layers, respectively;

etching the first and second masking layers to define first and second

mask patterns, respectively, the first and second mask patterns exposing regions of the first and second oxide layers, the exposed regions comprising first and second exposed regions of the first oxide layer and first exposed regions of the second oxide layer, the first mask pattern masking third and fourth regions of the first oxide layer and the second mask pattern masking second regions of the second oxide layer, the fourth regions of the first oxide layer being aligned with the second regions of the second oxide layer; and then

growing an oxide mask on the first and second exposed regions of the first and second oxide layers, the first and second mask patterns preventing the oxide mask from forming on the third and fourth regions of the first oxide layer and the second regions of the second oxide layer;

the batch processing steps comprising:

removing the first and second mask patterns to expose the third and fourth regions of the first oxide layer and the second regions of the second oxide layer;

removing the third and fourth regions of the first oxide layer and the second regions of the second oxide layer to expose first, second and third surface regions, respectively, of the cap wafer between portions of the oxide mask;

etching the first, second and third surface regions of the cap wafer,

wherein etching of the first surface regions of the cap wafer produces multiple recesses in the first surface of the cap wafer and etching of the second and third surface regions of the cap wafer produces multiple through-holes in the cap wafer; and then

removing the oxide mask and the first and second exposed regions of the first and second oxide layers thereunder; ~~to yield a cap wafer with multiple through-holes and recesses;~~

the method then further comprising the steps of:

mating the cap wafer with a device wafer so that the recesses of the cap wafer define cavities enclosing micromachined elements on the device wafer and the through-holes provide access to bond pads on the device wafer;

bonding the cap wafer to the device wafer to form a wafer stack; and then

singulating die from the wafer stack to produce the multiple MEMS device packages.

Claim 9 (Original): The method according to claim 8, wherein the first and second masking layers are formed of silicon nitride.

Claim 10 (Currently amended): The method according to claim 8,

wherein the cap wafer is a silicon wafer, the first and second oxide layers are silicon dioxide layers, and the oxide mask is formed of silicon dioxide grown by oxidizing the first and second exposed regions of the first oxide layer and the second exposed region of the second oxide layer.

Claim 11 (Currently amended): The method according to claim 8, wherein the step of etching the first, second and third surface regions of the cap wafer to produce the through-holes and the recesses is an anisotropic etch.

Claim 12 (Currently amended): The method according to claim 8, wherein a surface defect is present in at least one of the first and second mask patterns prior to the step of forming the oxide mask, the step of forming the oxide mask results in oxide forming in the defect, and the step of etching the first, second and third surface regions of the cap wafer causes the oxide in the defect to be undercut so as not to effect the sizes and shapes of the through-holes or recesses formed in the first, second and third surface regions of the cap wafer.